DETAILED ACTION

This Office Action is in response to Amendment filed October 6, 2009.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "offset region" recited in claims 1 and 7 must be shown or the feature canceled from the claims, because only LDD regions are shown in Figs. 5 and 6. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 5, 6, 11 and 12 are objected to because of the following informalities:

On line 3 of claims 5 and 11, "the" before "source and drain" should be removed to avoid indefiniteness.

On line 2 of claim 6, "offset regions" should be replaced by "offset region", because previously presented claim included "offset region" not "offset regions".

On line 3 of claim 12, "light" should be replaced by "lightly".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 3-5, 7 and 9-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Regarding claims 1 and 7, Applicants originally disclosed that "the width between "primary" crystal grain boundaries of polysilicon forming the activation layer 13 should be wider than that of the LDD region II" ([0036] of current Application), and originally claimed that "a width of an activation layer including the LDD region or offset region is shorter than a distance

between the primary crystal grain boundaries" in original claims 2 and 8. However, Applicants did not originally disclose that “a width of the offset region, included in an activation layer, is smaller than a distance between the primary crystal grain boundaries (emphasis added)” as recited in claims 1 and 7. Claims 3-5 depend on claim 1, and claims 9-11 depend on claim 7, and therefore claims 3-5 and 9-11 also fail to comply with the written description requirement.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 3-5, 7 and 9-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claims 1 and 7, it is not clear whether Applicants claim "an offset region having no doping", or an offset region not intentionally doped. Even though Applicants disclosed that "an offset region refers to a region that is not doped” in paragraph [0028] of current Application, a polysilicon layer formed from an amorphous silicon would *inherently* comprise impurities or dopants incorporated during a solidification process or from diffusion of dopants from nearby source and drain regions. Claims 3-5 depend on claim 1, and claims 9-11 depend on claim 7, and therefore claims 3-5 and 9-11 are also indefinite. In the below prior art rejections, it is interpreted that the “offset region” is not intentionally doped but still may be doped at a low doping concentration.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 3-7 and 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Oka et al. (US 6,184,541).

Regarding claims 1, 4, 5, 7, 10 and 11, Oka et al. disclose (a flat panel display device (col. 2, lines 27-29) comprising) a thin film transistor (TFT) (Figs. 1a and 1b) comprising an offset region (region between rightmost primary crystal grain boundary in channel region 8 and region 4) (no doping is disclosed for channel region 8) having no doping and a plurality of primary crystal grain boundaries (2) (boundaries substantially perpendicular to current direction) (col. 3, lines 36-37), wherein the thin film transistor is formed so that the primary crystal grain boundaries (2) of a polysilicon substrate (3) (col. 3, line 36) are not positioned in the offset region, and wherein a width of the offset region (region between rightmost primary crystal grain boundary in channel region 8 and region 4), included in an activation layer (composite layer of 6, 7 and 8) (col. 3, lines 42-43), is smaller than a distance between the primary crystal grain boundaries (2) (for example, a distance between two primary crystal grain boundaries wherein one primary crystal grain boundary is selected from each region 5) (claims 1 and 7), wherein the thin film transistor may be used in an LCD device (col. 2, lines 27-29) (claims 4 and 10), and the primary crystal grain boundaries (2) are substantially perpendicular to a current

direction between source and drain regions (6 and 7, respectively) of the thin film transistor (claims 5 and 11).

Regarding claims 3 and 9, the limitation "the polysilicon substrate is formed by a sequential lateral solidification (SLS)" is merely a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966.

Regarding claim 6, Oka et al. disclose a thin film transistor (TFT) (Figs. 1a and 1b) comprising a lightly doped drain (LDD) region or offset region (portion of region 4 included in width "d" on the right side) (col. 3, lines 60-66, and col. 4, lines 63-66) and a plurality of primary crystal grain boundaries (2) (col. 3, lines 36-37), wherein the thin film transistor is formed so that the primary crystal grain boundaries (2) of a polysilicon substrate (3) (col. 3, line 36) are positioned in channel, source and drain regions (8 and two regions denoted as 5) (col. 3, lines 42 and 39-40) but not positioned in the LDD or offset region (portion of region 4 included in width "d" on the right side), and wherein a width (d) of the LDD region or offset region is less than a distance between two adjoining primary crystal grain boundaries (one rightmost primary crystal grain boundary in channel region 8 and another leftmost primary crystal grain boundary in region 4 on the right) as clearly shown in Fig. 1(a).

Regarding claim 12, Oka et al. disclose a flat panel display device (col. 2, lines 27-29) comprising a thin film transistor (Figs. 1a and 1b) comprising a lightly doped drain (LDD) region or offset region (portion of region 4 included in width "d" on the right side) (col. 3, lines 60-66, and col. 4, lines 63-66), and a plurality of primary crystal grain boundaries (2) (col. 3, lines 36-37), wherein the thin film transistor (Figs. 1a and 1b) is formed so that the primary crystal grain boundaries (2) of a polysilicon substrate (3) (col. 3, line 36) are positioned in channel, source and drain regions (8 and two regions denoted as 5) (col. 3, lines 42 and 39-40) but not positioned in the LDD or offset region (portion of region 4 included in width "d" on the right side), and wherein a width (d) of the LDD region or offset region is less than a distance between two adjoining primary crystal grain boundaries (one rightmost primary crystal grain boundary in channel region 8 and another leftmost primary crystal grain boundary in region 4 on the right) as clearly shown in Fig. 1(a).

Response to Arguments

9. Applicants' arguments, see REMARKS, filed October 6, 2009, with respect to 35 USC 102 rejection, referring to a portion of 4 with a width d in Oka et al. as an offset region having no doping, have been fully considered and are persuasive. The 35 USC 102 rejection of claims 1 and 7 using this interpretation has been withdrawn. However, the 35 USC 102 rejection of claims 1 and 7 referring to a region between rightmost primary crystal grain boundary in channel region 8 and region 4 in Fig. 1a of Oka et al. as an offset region having no doping is maintained.

10. Applicants' arguments filed October 6, 2009 have been fully considered but they are not persuasive.

Applicants argue that “[a]s noted in the description of FIG. 5 in paragraph [0030] of the specification, it is disclosed that a thin film transistor includes an offset region or an LDD region, and it is disclosed that region II of FIG. 5 is referred to as an LDD region in the detailed description of the drawing”, and that “[h]owever, item II in FIG. 5 can also be an offset region”. The latter argument is contradictory to Applicants’ original disclosure in [0028] of current Application, which states that "[f]urthermore, off current, that is, leakage current, can be reduced in a thin film transistor by adding an LDD region to the offset region through low density ion doping of impurities (emphasis added)", which clearly suggests that an offset region and an LDD region are different and separate regions. Further, Applicants admit on page 8 of REMARKS filed October 6, 2009 that “[f]urthermore, as noted above, Applicants note that "the offset region" is known to one of ordinary skill in the art as being completely different from "the LDD region" in terms of technology, and thus "the offset region" is not referred to as "the LDD region". In other words, Applicants admit that an LDD region and an offset region are completely different but *also* argue that the LDD region shown in Fig. 5 of current Application can be replaced by an offset region.

Applicants argue that “[i]n other words, item II of FIG. 5 refers to either an LDD region or an offset region”, and that “[a]ccordingly, as noted above, since the LDD region can be replaced by the offset region, the specification clearly provides proper support for the recitation that a width of the offset region included in the activation layer

is smaller than a distance between the primary crystal grain boundaries". See the above responses.

Applicants argue that "[a]s noted at page 3 of the Non-Final Office Action mailed on July 6, 2009, the Examiner states that Applicants disclosed that the width between primary crystal grain boundaries should be wider than that of the LDD region, and that a width of the LDD region or the offset region is shorter than a width between primary crystal grain boundaries (emphasis added)". The underlined portion is *only* a portion of what the Examiner stated. The Examiner clearly stated that original claims recited "a width of an activation layer including the LDD region or offset region is shorter than a distance between the primary crystal grain boundaries".

Applicants argue that "Applicants note that "the offset region" refers to a region into which impurities are not doped, other than a channel region in an active layer formed of polysilicon", and that "[t]herefore, such a term is a general term which is commonly used in the field and one or ordinary skill in the art would readily recognize the term and its definition". (1) Applicants do not disclose where the claimed offset region is located in Drawings. (2) Applicants do not specifically claim whether the offset region has no impurities at all, which may not be enabling because impurities such as hydrogen or carbon would be *inherently* incorporated during a recrystallization process, or the offset region is undoped but still may be doped unintentionally. In other words, do Applicants really claim 100% pure silicon, which may not be enabling, for the claimed offset region? (3) Applicants do not disclose or claim that the offset region is located in a region other than a channel region. Also, Applicants do not specifically disclose or

claim what the offset region does. (4) Dictionary.com defines "offset" as "placed away from a center line" or "off-center", and therefore a region between rightmost primary crystal grain boundary of channel region 8 and region 4 in Fig. 1a of Oka et al. may also be referred to as an "offset" region. (5) Claims must be given their broadest reasonable interpretation. See MPEP 2111.

The Examiner notes that Applicants did not respond to 35 USC 102 rejection of claims 1 and 7 referring to a region between rightmost primary crystal grain boundary in channel region 8 and region 4 in Fig. 1a of Oka et al. as an offset region.

Applicants argue that "[r]egarding the rejection of independent claims 6, 7 and 12, it is noted it is noted [sic] that these claims recite some substantially similar features as claim 1". Independent claims 6 and 12 are completely different in scope from independent claims 1 and 7 in that a lightly doped drain (LDD) region is recited in claims 6 and 12.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571) 270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Examiner, Art Unit 2815
January 7, 2010
/Kenneth A Parker/
Supervisory Patent Examiner, Art Unit 2815